

said system control means comprises:

a collective-type means-basis ECC block pipeline processing notification sub means for collectively transmitting ECC blocks which have been subjected to error correction downstream; for collectively storing ECC blocks to be processed next to said plural-ECC-block-division buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a collective-type means-basis ECC block code word recognition sub means for selecting code words of the ECC blocks to be processed, in accordance with the contents stored in said ECC-block-and-code word-division storing means, in controlling a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; in controlling the error correction done by said error correcting means; in controlling writing of error-corrected data to said ECC-block-basis buffer memory done by said bus control means; in storing mid-term results to said ECC-block-and-code word-division storing means by said error detecting means; and

a collective-type ECC block notification sub means in sub means-basis pipeline processing for notifying said first error detecting sub means, said even-numbered error correction sub means, said odd-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means contained in said system control means that the error-corrected ECC blocks have been collectively

blocks to be processed next to said plural-ECC-block-division buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

5 a collective-type means-basis ECC block code word recognition sub means for selecting code words of the ECC blocks to be processed, in accordance with the contents stored in said ECC-block-and-code word-division storing means, in controlling a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error
10 correction; in controlling the error correction done by said error correcting means; in controlling writing of error-corrected data to said ECC-block-basis buffer memory done by said bus control means; in storing mid-term results to said ECC-block-and-code word-division storing means
15 by said error detecting means; and

a collective-type ECC block notification sub means in sub means-basis pipeline processing for notifying said first error detecting sub means, said even-numbered error correction sub means, said odd-numbered error correction sub means, said number-of-times control sub means, and said
20 DMA transfer instruction sub means contained in said system control means that the error-corrected ECC blocks have been collectively transmitted downstream and new ECC blocks to be processed have been collectively stored in said plural-ECC-block-division buffer memory, and further notifying these same sub means contained in said system control
25 means of the ECC blocks which are in process therein.